ADLINK TECHNOLOGY INC.

LittleBoard™ 735
Single Board Computer
Reference Manual

P/N 50-1Z020-1000

Notice Page

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REVISION HISTORY

Revision	Reason for Change	Date
00	Initial Release	April/09

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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

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Chapter 1 About This Manual

Purpose of this Manual

This manual is for designers of systems based on the LittleBoard™ 735 single board computer (SBC). This manual contains information that permits designers to create an embedded system based on specific design requirements.

Information provided in this reference manual includes:

- LittleBoard 735 specifications
- Environmental requirements
- Major integrated circuits (chips) and features implemented
- LittleBoard 735 connector/pin numbers and definitions
- BIOS Setup information

Information not provided in this reference manual includes:

- Detailed chip specifications
- Internal component operation
- Standard connector pin-out tables
- Internal registers or signal operations
- Bus or signal timing for industry standard busses and signals

References

The following list of references may be helpful for you to complete your design successfully. Most of these references are also available on the Ampro By ADLINK web site in the InfoCenter. The InfoCenter was created for embedded system developers to share ADLINK's knowledge, insight, and expertise.

Specifications:

- EBX Spec Revision 2.0, March 1, 2005

  For the latest version of the EBX specifications, contact the PC/104 Consortium, at:

  Web site: http://www.pc104.org

- PCI Express Mini Card Spec Revision 1.0

  For latest revision of the PCI Express Mini Card specifications, contact the PCI Special Interest Group Office, at:

  Web site: http://www.pcisig.com/specifications/pciexpress/mini

- PC/104 Spec Revision 2.5, November 2003
- PC/104-Plus Spec Revision 2, November 2003

  For latest revision of the PC/104 specifications, contact the PC/104 Consortium, at:

  Web site: http://www.pc104.org

- PCI 2.2 Compliant Specifications

  For latest revision of the PCI specifications, contact the PCI Special Interest Group Office at:

  Web site: http://www.pcisig.com

Chip specifications used on the LittleBoard 735:

- Intel Corporation and the Atom N270 processor used for the embedded CPU.

  Web site: http://download.intel.com/design/processor/datashts/320032.pdf

- Intel Corporation and the 82945GSE and 82801GBM chips, used for the Memory Hub/Video controller and I/O Hub, respectively.

  Web site: http://download.intel.com/design/processor/datashts/309219.pdf = Memory Hub

  Web site: http://www.intel.com/Assets/PDF/datasheet/307013.pdf = I/O Hub

- Intel Corporation and the 82562GT and 82574IT chips, used for the Fast Ethernet and Gigabit Ethernet controllers, respectively.

  Web site: http://download.intel.com/design/network/datashts/82562gt.pdf = Ethernet

  Web site: http://download.intel.com/design/network/datashts/82574.pdf = Gigabit Ethernet

- Standard Microsystems Corp and the SCH3114I-NU chip, used for the Super I/O controller.

  Web site: http://www.smsc.com/main/catalog/sch311x.html

- Realtek and the ALC203 chip, used for the Audio CODEC.

  Web site: http://www.realtek.com.tw/search/default.aspx?keyword=ALC203

- ITE Tech. Inc. and the IT8888F chip, used for the PCI-to-ISA bridge conversion.

  Web site: http://www.ite.com.tw/EN/products_more.aspx?CategoryID=3&ID=5,76

NOTE	If you are unable to locate the datasheets using the links provided, go to the manufacturer's web site where you should be able to perform a search using the chip datasheet number or name listed, including the extension, htm, pdf, etc.

Chapter 2 Product Overview

This introduction presents general information about the EBX architecture and the LittleBoard 735 single board computer (SBC). After reading this chapter you should understand:

- EBX Architecture
- LittleBoard 735 Description
- LittleBoard 735 Features
- Block Diagram
- Major Components
- Headers and Connectors
- Jumper Headers
- Specifications (physical, environmental, power, cooling)

EBX Architecture

The “Embedded Board, eXpandable” (EBX) standard is the result of a collaboration between industry leaders, Motorola and Ampro, to unify the embedded computing industry through a full featured embedded single-board computer (SBC) standard. The EBX standard principally defines physical size, mounting hole pattern, and power connector locations. It does not specify processor type or electrical characteristics. There are recommended connector placements for serial/parallel, Ethernet, graphics, and memory expansion.

Derived from the Ampro LittleBoard form-factor originated in 1984, EBX combines a standard footprint with open interfaces. The EBX form-factor is small enough for deeply embedded applications, yet large enough to contain the functions of a fully embedded SBC (single board computer) including CPU, memory, mass storage interfaces, display controller, serial/parallel ports, today’s advanced operating systems, and other system functions. This embedded SBC standard ensures that embedded system OEMs can standardize their designs and that embedded computing solutions can be designed into space constrained environments with off-the-shelf components.

The EBX standard boasts highly flexible and adaptable system expansion, allowing easy and modular addition of functions such as additional USB 2.0 ports, Firewire or wireless networking not usually contained in standard product offerings. The EBX system expansion is based on popular existing industry standards, PC/104™ and PC/104-Plus™. PC/104 places the ISA bus on compact 3.6" x 3.8" modules with self-stacking capability. PC/104-Plus adds the power of a PCI bus to PC/104 while retaining the basic form-factor. Using PC/104 expansion cards, the PC/104 standard offers access to PC cards from the mobile and handheld computing markets.

The EBX standard integrates all these off-the-shelf standards into a highly embeddable SBC form-factor. EBX supports the legacy of PC/104, hosting the wide variety of embedded system oriented expansion modules from hundreds of companies worldwide. PC/104 brings the advantages of the latest portable and mobile system expansion technologies to embedded applications. See Figure 2-1 on page 4.

The EBX standard also brings stability to the embedded board market and offers OEMs assurance that a wide range of products will be available from multiple sources – now and in the future. The EBX standard is open to continuing technology advancements since it is processor independent. It creates opportunity for economies of scale in chassis, power supply, and peripheral devices.

The EBX specification is freely available to all interested. For further technical information on the EBX standard, go to the PC/104 Consortium web site at www.pc104.org.

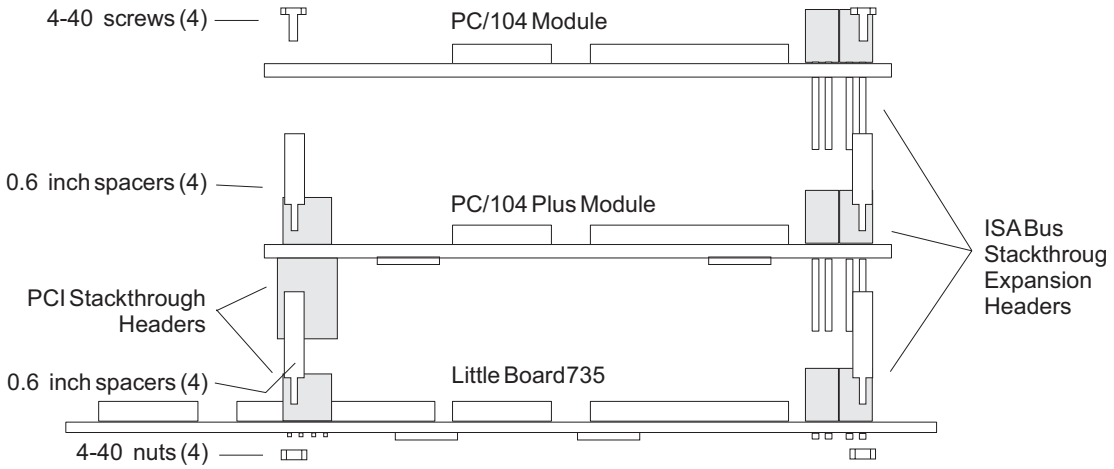

Figure 2-1. Stacking PC/104 Modules with the LittleBoard 735

Product Description

The LittleBoard 735 is an exceptionally high integration, high performance, rugged, and high quality single-board system, which contains all the component subsystems of a PC motherboard plus the equivalent of up to 3 expansion boards. Based on the Intel Atom N270 low power, high-integration processor, the LittleBoard 735 gives designers a complete, high performance, embedded processor based on the EBX form factor and conforms to the EBX V2.0 specifications.

Each LittleBoard 735 incorporates an Intel 945GSE chipset for the Graphics and Memory Hub (Northbridge) and the I/O Hub (Southbridge) controllers. This set includes the 82945GSE, Graphics and Memory Controller Hub, (also GMCH), which controls the graphics and memory interface. The other chip in this set is the 82801GBM, I/O Controller Hub 7 Mobile (ICH7-M), which controls some of the I/O functions on the board. One additional chip provides the remainder of the I/O functions: the Standard Microsystems, SCH3114I-NU, Super I/O controller. Together the Intel and SMSC chips provide four serial ports, an EPP/ECP parallel port, six USB 2.0 ports, PS/2 keyboard and mouse interfaces, floppy, one Ultra/DMA 33/66/100 IDE controller supporting Compact Flash, independent 10/100BaseT and 10/100/1000BaseT Ethernet interfaces, an audio AC'97 CODEC, PCIe Mini Card, GPIO, SMBus, and two SATA ports on the board. To provide the ISA bus on the board through the PC/104 connector, an ITE IT8888G-L, PCI-to-ISA Bridge is included. The LittleBoard 735 also supports up to 2GB of DDR2 RAM in a single 200-pin SODIMM slot, and a Graphics Media Accelerator (GMA), which provides CRT, TV Out, and LVDS flat panel video interfaces for most popular LCD panels.

The LittleBoard 735 can be expanded through the PC/104 and PC/104-Plus expansion for additional system functions, as these buses offer compact, self-stacking, modular expandability. The PC/104 and PC/104-Plus buses are the embedded system version of the signal set provided on a desktop PC's ISA and PCI buses at 8MHz and 33MHz clock speeds, respectively.

Among the many embedded-PC enhancements on the LittleBoard 735 that ensure embedded system operation and application versatility are a watchdog timer, serial console support, battery-free boot, on-board, high-density Compact Flash socket, and BIOS extensions for OEM boot customization.

The LittleBoard 735 is particularly well suited to either embedded or portable applications and meets the size, power consumption, temperature range, quality, and reliability demands of embedded system applications. It can be stacked with ADLINK MiniModules™ or other PC/104-compliant expansion boards, or it can be used as a powerful computing engine.

Board Features

- CPU features
  - Intel 1.6GHz LV, Atom N270 Processor
  - 512KB L2 cache
  - 533MHz FSB
- Memory
  - Single standard 200-pin DDR2 SODIMM socket
  - Supports non-ECC, unbuffered memory
  - Supports +2.5V DDR2, 533MHz RAM up to 2GB
- PC/104-Plus Bus Interfaces
  - PCI Bus up to 33MHz
  - PCI 2.2 compliant signals
  - PC/104 (ISA) Bus up to 8MHz
- IDE Interfaces
  - Provides one enhanced IDE controller (Compact Flash)
  - Supports Ultra DMA 33/66/100 modes
  - Supports ATAPI and DVD peripherals
  - Supports IDE native and ATA compatibility modes
- Floppy Disk Interface
  - Supports one standard floppy disk drive interface
  - Supports all standard PC/AT formats: 360KB, 1.2MB, 720KB, 1.44MB, 2.88MB
- Parallel Port
  - Provides a standard printer interface
  - Supports IEEE standard 1284 protocols of EPP and ECP outputs
  - Supports Bi-directional data lines
  - Supports 16 byte FIFO for ECP mode
- Serial Ports
  - Four buffered serial ports with full handshaking
  - Provides 16550-equivalent controllers, each with a built-in 16-byte FIFO buffer
  - Supports full modem capability on all four ports
  - Supports RS232, RS485, or RS422 operation on each port
  - Supports programmable word length, stop bits, and parity
  - Supports 16-bit programmable baud-rate generator and an interrupt generator
- USB Ports
  - Provides three root USB hubs
  - Provides up to six USB ports
  - Supports USB boot devices
  - Supports USB v2.0 EHCI and UHCI v1.1

- Supports over-current detection status

- Keyboard/Mouse Interface
  - Provides PS/2 keyboard interface
  - Provides PS/2 mouse interface
- Audio interface
  - Provides AC'97 CODEC on board
  - Supports AC'97 standard
- Ethernet Interface
  - Provides two fully independent Ethernet ports
  - Provides integrated LEDs on each port (Link/Activity and Speed)
  - Provides Intel 82562GT and 82574IT controller chips
  - Supports IEEE 802.3 10/100BaseT and 10/100/1000BaseT compatible physical layers
  - Supports Auto-negotiation for speed, duplex mode, and flow control
  - Supports full duplex or half-duplex mode
    - Full-duplex mode supports transmit and receive frames simultaneously
    - Supports IEEE 802.3x Flow control in full duplex mode
    - Half-duplex mode supports enhanced proprietary collision reduction mode
- Video Interfaces (CRT/LVDS/TV Out)
  - Support CRT (2048 x 1536) with up to 64MB UMA (Unified Memory Architecture)
  - AGP 4X equivalent graphics performance
  - Dual channel 9-, 12-, or 18-bit LVDS
  - LVDS outputs (1 or 2 channel, four differential signals: 3-bits + clock)
  - Provide one TV Out header
- Miscellaneous
  - Real-time clock (RTC) with replaceable battery
  - Battery-free boot (Boots even if battery is dead or missing)
  - Supports both on-board or external battery for Real Time Clock operation
  - Thermal and Voltage monitoring
  - Oops! Jumper (BIOS recovery) support
  - Serial Console
  - Watchdog timer (WDT)

Block Diagram

Figure 2-2 shows the functional components of the board.

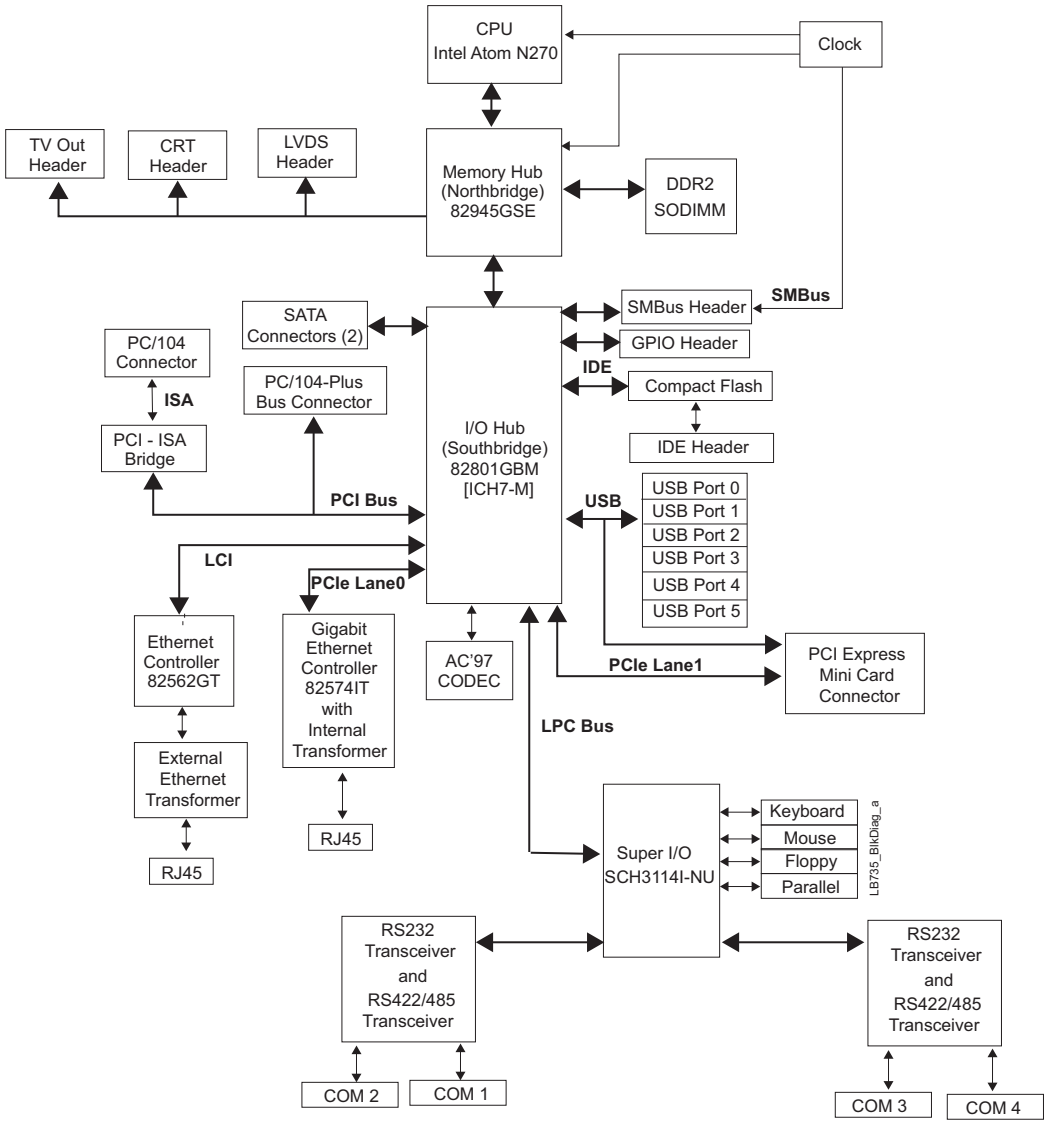

Figure 2-2. Functional Block Diagram

Major Components (ICs)

Table 2-1 on page 8 lists the major ICs on the LittleBoard 735, including a brief description of each. Figures 2-3 and 2-4 show the locations of the chips.

Table 2-1. Major Integrated Circuit Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	Intel	Atom N270	CPUs offered at 1.6GHz	Embedded CPU
Memory Hub (U2)	Intel	82945GSE	Northbridge Memory and Video controller	Memory and Video
I/O Hub (U4)	Intel	82801GBM (ICH7-M)	Southbridge I/O controller	I/O Functions
Super I/O (U15 on back of the board) [See Figure 2-4]	SMC	SCH3114I-NU	Remaining I/O controller	I/O Functions
Ethernet Controller (U10)	Intel	82574IT	10/100/1000BaseT Gigabit Ethernet controller	LAN0 Ethernet Function
Ethernet Controller (U12)	Intel	82562GT	10/100BaseT Fast Ethernet controller	LAN1 Ethernet Function
ISA Bridge (U13)	ITE	IT8888F	PCI-to-ISA bridge	ISA Bus
Audio AC'97 CODEC (U14)	Realtek	ALC203-LF	Audio AC'97 CODEC for audio signals	Audio In/Out
RS232 Transceiver (U17)	Maxim	MAX213ECAI+	RS232 Transceiver for COM1 and COM2	Serial Ports 1 and 2 Transceiver
RS485/422 Transceiver (U19)	Linear	LTC1334CG#PBF	RS422/485 Transceiver for COM1 and COM2	Serial Ports 1 and 2 Transceiver
RS232 Transceiver (U21)	Maxim	MAX213ECAI+	RS232 Transceiver for COM3 and COM4	Serial Ports 3 and 4 Transceiver
RS485/422 Transceiver (U22)	Linear	LTC1334CG#PBF	RS422/485 Transceiver for COM3 and COM4	Serial Ports 3 and 4 Transceiver
Ethernet Transformer (U25)	Pulse	H1102NLT	Fast Ethernet Transformer	Ethernet Magnetics

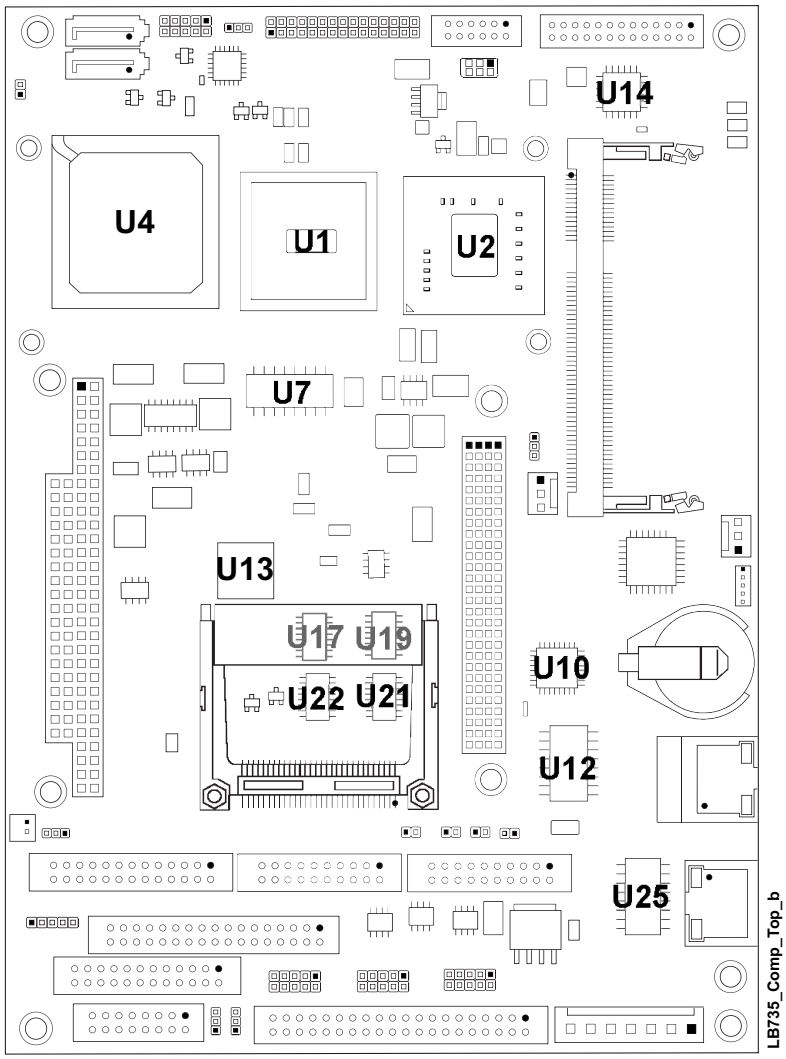

Figure 2-3. Component Locations (Front view)

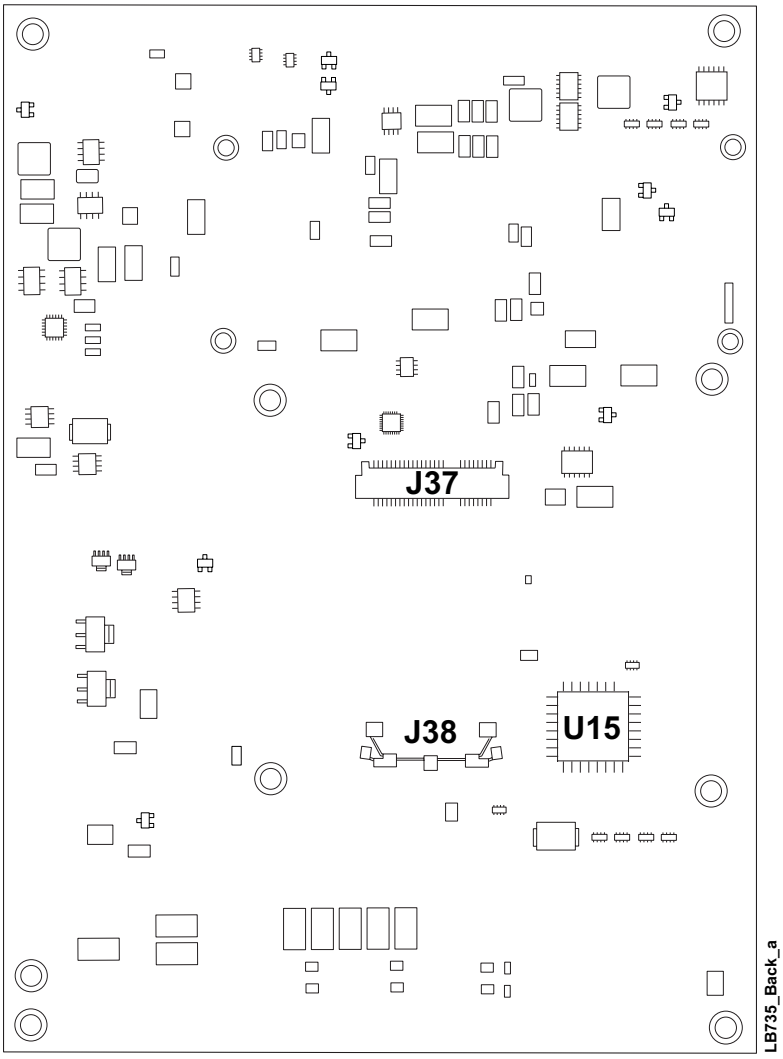

Figure 2-4. Component Locations (Back view)

Headers and Connectors

Table 2-2 describes the headers and connectors shown in Figure 2-6 on page 13. All I/O headers use 0.100" (2.54mm) pitch unless otherwise indicated.

Table 2-2. Header and Connector Descriptions

Jack #	Name	Description
BAT1	Battery Socket	Battery socket for 3 volt Lithium battery
J1A,B, C,D	PC/104 bus	104-pin standard connector for PC/104
J2A,B, C,D	PC/104-Plus	120-pin, 0.079" (2mm), standard connector for PCI bus
J3	Video (CRT)	12-pin, 0.079" (2mm), header for output to a CRT type monitor
J6	IDE	40-pin standard header for the primary IDE interface

Table 2-2. Header and Connector Descriptions (Continued)

J8	Compact Flash	50-pin, 0.050" (1.27mm), socket accepts Type I or Type II Compact Flash cards
J9	Audio In/Out	26-pin, 0.079" (2mm), header for all of the audio signals (input/output)
J10	LAN1	8-pin, RJ45 connector for 10/100/1000BaseT Gigabit Ethernet port with magnetics
J11	Serial A	20-pin header for serial ports 1 and 2 (COM 1 & COM 2)
J12	Serial B	20-pin header for serial ports 3 and 4 (COM 3 & COM 4)
J13	Utility 2	24-pin header for mouse, SMBus, and power button
J14	USB 2 & 3	10-pin, 0.079" (2mm) header for USB2 and USB3 ports
J15	Utility 1	16-pin header for keyboard, external battery, reset switch, and speaker
J16	Parallel	26-pin header for parallel port
J17	Floppy	34-pin header for floppy disk drive interface
J19	Power In	7-pin, 0.156" (3.96mm), header for input power
J23	LAN2	8-pin, RJ45 connector for 10/100BaseT Fast Ethernet port
J26	Video (LVDS)	30-pin, 0.079" (2mm), header for LVDS type video displays
J30	Power On	3-pin header for ATX power-on functions
J31	Memory	200-pin, 0.024" (0.60mm) socket for DDR2 SDRAM SODIMM
J32	SATA1	7-pin, 0.050" (1.27mm) standard connector for serial ATA
J33	SATA2	7-pin, 0.050" (1.27mm) standard connector for serial ATA
J34	Optional Fan	3-pin header provides +5V or +12V, tach, and ground to optional CPU fan
J35	Battery Input	2-pin, 0.049" (1.24mm) header for power from external battery
J36	TV Out	6-pin header for TV Out signals
J37	PCI Express Mini Card (on back of the board; see Figure 2-4 on page 10)	52-pin, 0.012" (0.30mm) standard socket for PCI Express Mini Card functions
J38	Latch (on back of the board; see Figure 2-4 on page 10)	Latch for the PCI Express Mini Card connector
J39	USB 4 & 5	10-pin, 0.079" (2mm) header for USB4 and USB5 ports
J40	GPIO	10-pin, 0.079" (2mm) header for General Purpose IO signals
J41	DNP	Do not populate
J43	DNP	Do not populate
J44	USB 0 & 1	10-pin, 0.079" (2mm) header for USB0 and USB1 ports
J45	SMBus	5-pin, 0.049" (1.25mm) header for external device connection
J46	Power On Button and Reset Switch	5-pin header for power-on button and reset switch

NOTE The pinout tables in Chapter 3 of this manual identify pin sequence using the following methods: A 20-pin header with two rows of pins, using odd/even numbering, where pin 2 is directly across from pin 1, is noted as 20-pin, 2 rows, odd/even (1, 2). Alternately, a 20-pin connector using consecutive numbering, where pin 11 is directly across from pin 1, is noted in this way: 20-pin, 2 rows, consecutive (1, 11). The second number in the parenthesis is always directly across from pin 1. See Figure 2-5.

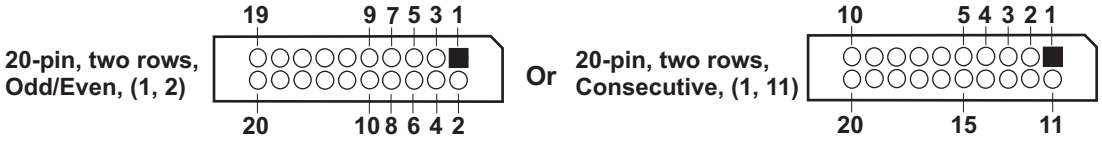

Figure 2-5. Pin Sequence Identification

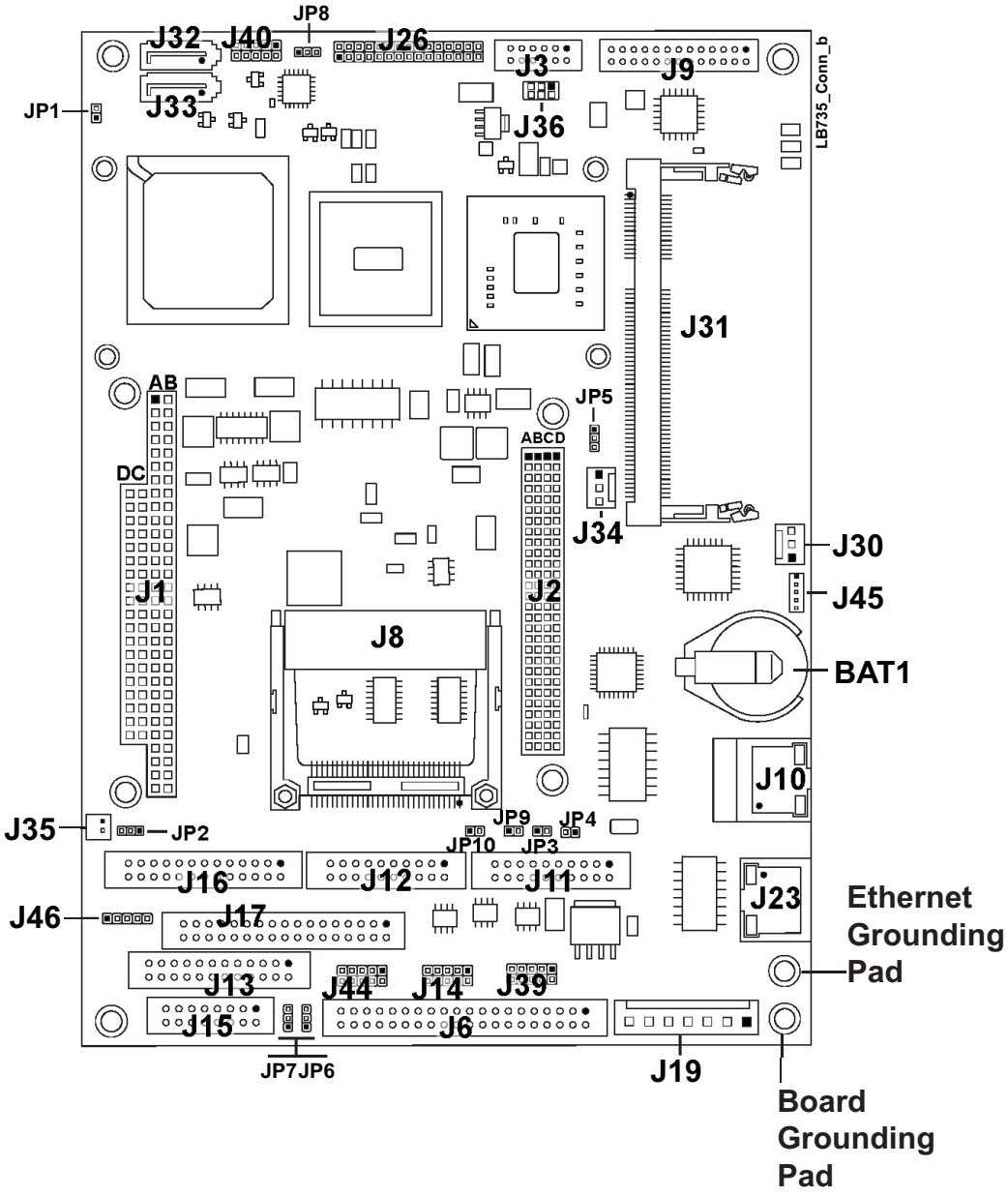

Figure 2-6. Connector Locations (Top view)

CAUTION	The two Ethernet ports share a common ground (transformer center tap), that is floating until you determine how the common ground is connected. The grounding holes (8) of the LittleBoard 735 are connected to ground potential (return) of the DC power supply connected to the board through J19.

NOTE	Pin 1 is shown as a black pin (square or round) on all headers in all illustrations.

Jumper Header Definitions

Table 2-3 describes the jumper headers shown in Figure 2-6 on page 13.

Table 2-3. Jumper Settings

Jumper #	Installed	Removed/Installed
JP1 – RTC (Real Time Clock) Reset	Enable (pins 1-2)	Disable (Removed) **Default**
JP2 – Power Management	Power Up by S3 (pins 1-2) **Default**	Power Up by S5 (pins 2-3)
JP3 – Serial Port 2 RS485 Termination	Enable Termination (pins 1-2)	Disable Termination (Removed) **Default**
JP4 – Serial Port 1 RS485 Termination	Enable Termination (pins 1-2)	Disable Termination (Removed) **Default**
JP5 – Fan Voltage Selection	Enable +5V (pins 1-2)	Enable +12V (pins 2-3) **Default**
JP6 – Compact Flash Master/Slave	Enable Slave (pins 1-2) **Default** [ATA Master]	Enable Master (pins 2-3) [ATA Slave]
JP7 – Compact Flash Voltage Selection	Enable +5V (pins 1-2)	Enable +3.3V (pins 2-3) **Default**
JP8 – LVDS Voltage Selection	Enable +3.3V (pins 1-2) **Default**	Enable +5V (pins 2-3)
JP9 – Serial Port 4 RS485 Termination	Enable Termination (pins 1-2)	Disable Termination (Removed) **Default**
JP10 – Serial Port 3 RS485 Termination	Enable Termination (pins 1-2)	Disable Termination (Removed) **Default**

Note: Only the jumper headers listed above are populated on the board. Jumpers or shunts use .079" (2mm) pitch.

Specifications

Physical Specifications

Table 2-4 lists the physical dimensions of the board.

Table 2-4. Weight and Footprint Dimensions

Item	Dimension
Weight	0.280kg. (0.60lbs.)
Height (overall)	16.26mm (0.64")
Width	146mm (5.75")
Length	203mm (8.0")
Thickness	2.36mm (0.093")

NOTE Overall height is measured from the upper board surface to the highest permanent component (J10, RJ45 connector) on the upper board surface. This measurement does not include the various heatsinks on the board. The heatsinks could increase this dimension.

Environmental Specifications

Table 2-5 provides the most efficient operating and storage condition ranges required for this board.

Table 2-5. Environmental Requirements

	Parameter	1.6GHz Atom N270 Conditions
Temperature	Operating	-20° to +70°C (-4° to +158°F)
	Extended (Optional)	–40° to +85°C (–40° to +185°F)
	Storage	–55° to +85°C (–67° to +185°F)
Humidity	Operating	5% to 95% relative humidity, non-condensing
	Non-operating	5% to 95% relative humidity, non-condensing

Power Specifications

Table 2-6 shows the power requirements from the baseboard and the board power output.

Table 2-6. Power Supply Requirements

Parameter	1.6GHz Atom N270 Characteristics
Input Type	Regulated DC voltages
In-rush Current	6.59A (32.95W)
Idle Power	1.09A (5.46W)
BIT Current	2.36A (11.78W)

Operating configurations:

- In-rush operating configuration includes video, 2GB DDR2 RAM, and power.
- Idle operating configuration includes the in-rush configuration as well as one IDE hard drive, I/O board, keyboard, and mouse.
- BIT = Burn-In-Test. Operating configuration includes idle configuration as well as two SATA hard drives, one on-board Compact Flash, one floppy drive, four serial loop-backs, one parallel loop-back, two Ethernet connections, four USB loop-backs, one USB flash drive, and one Compact Flash reader with 64MB Compact Flash.

Thermal/Cooling Requirements

The CPU, Memory Hub, I/O Hub, and voltage regulators are the sources of heat on the board. The LittleBoard 735 is designed to operate at the maximum speed of the CPU: 1.6GHz. The Atom N270 CPU requires a heatsink but no fan for -40°C to +85°C operation.

Mechanical Specifications

Figure 2-7 shows the top view of the LittleBoard 735 with the mechanical mounting dimensions.

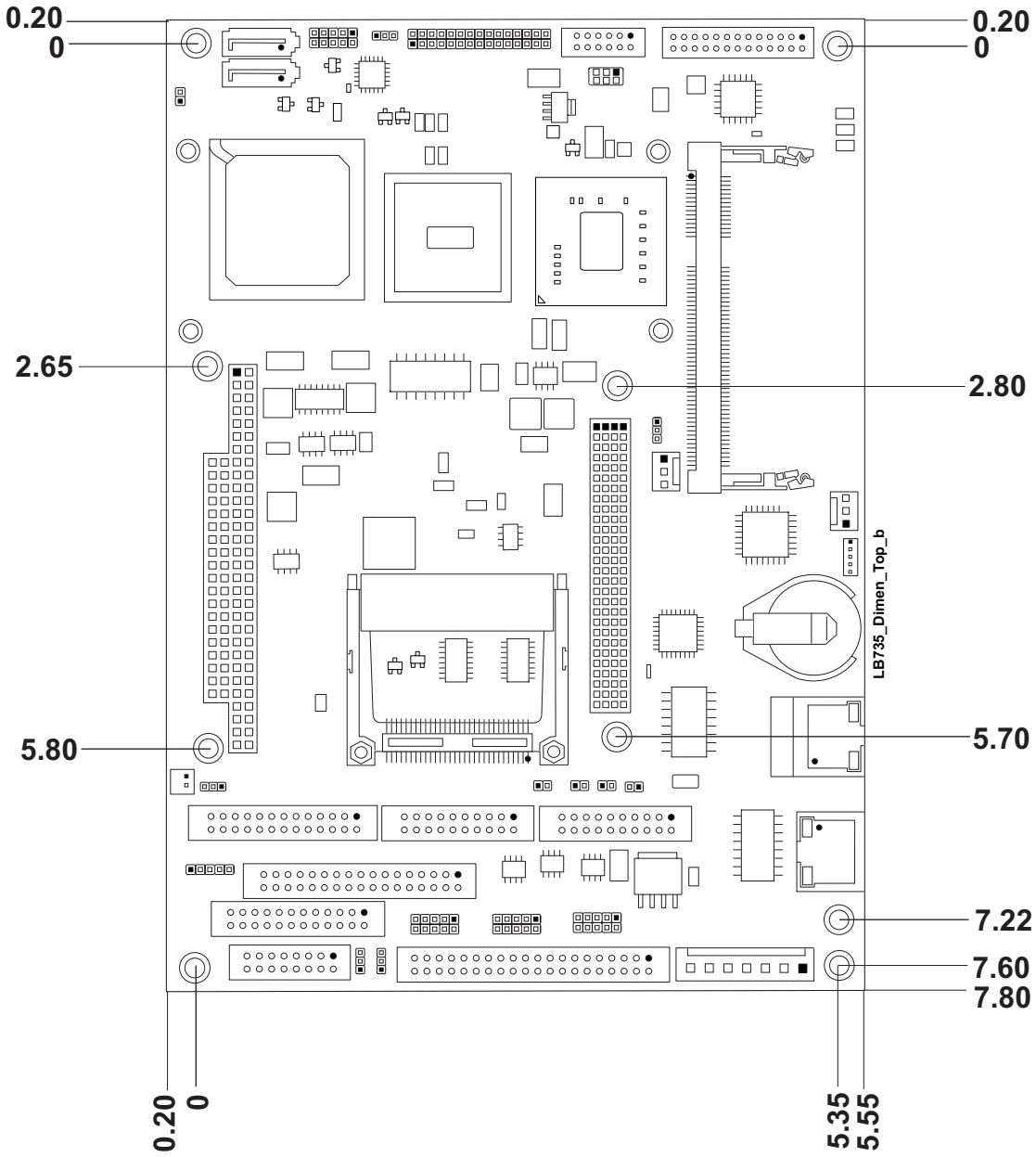

Figure 2-7. LittleBoard 735 Dimensions

NOTE	All dimensions are given in inches.

Chapter 3 Hardware

Overview

This chapter discusses the following features of the connectors:

- Interrupt Channel Assignments
- Memory Map
- I/O Address Map
- Floppy Interface
- Parallel Interface
- Serial Interfaces
- Utility Interfaces
  - Keyboard
  - Mouse
  - Battery
  - Reset Switch
  - Speaker
  - SMBus
- USB Interfaces
- Audio Interface
- Video Interfaces
  - CRT
  - LVDS
  - TV Out
- Power Interfaces
  - Power In
  - ATX Power
  - Power-On Button
- Miscellaneous
  - Time of Day/RTC
  - Temperature Monitoring
  - User GPIO Interface
  - SMBus Interface
  - Oops! Jumper (BIOS recovery)
  - Serial Console
  - Watchdog timer
  - Optional CPU fan
  - External Battery Input

NOTE ADLINK Technology, Inc. only supports the features/options tested and listed in this manual. The main integrated circuits (chips) used in the LittleBoard 735 may provide more features or options than are listed for the LittleBoard 735, but some of these chip features/options are not supported on the board and may not function as specified in the chip documentation.

This chapter does not include pinout tables for standard headers and connectors such as PC/104, Ethernet RJ45, 40-pin IDE, Floppy, and Compact Flash.

Interrupt Channel Assignments

The interrupt channel assignments are shown in Table 3-1.

Table 3-1. Interrupt Channel Assignments

Device vs IRQ No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer	X															
Keyboard		X														
Secondary Cascade			X													
COM1				O	D						O	O				
COM2				D	O						O	O				
COM3				O	O						O	D				
COM4				O	O						D	O				
Floppy							X									
Parallel						O		D							O	O
RTC									X							
IDE															D	
Math Coprocessor														X		
PS/2 Mouse													X			
PCI INTA				O	O	D	O	O		O	O	O	O		O	O
PCI INTB				O	O	O	O	O		D	O	O	O		O	O
PCI INTC				O	O	D	O	O		O	O	O	O		O	O
PCI INTD				O	O	O	O	O		D	O	O	O		O	O
PCI INTE				O	O	D	O	O		O	O	O	O		O	O
PCI INTF				O	O	O	O	O		D	O	O	O		O	O
PCI INTG				O	O	D	O	O		O	O	O	O		O	O
PCI INTH				O	O	O	O	O		D	O	O	O		O	O

Legend: D = Default, O = Optional, X = Fixed

NOTE The IRQs for the Ethernet, Video, and Internal Local Bus (ISA) are automatically assigned by the BIOS Plug and Play logic. Local IRQs assigned during initialization can not be used by external devices.

Memory Map

The following table provides the common PC/AT memory allocations. Memory below 000500h is used by the BIOS.

Table 3-2. Memory Map

Base Address			Function
00000000h	-	0009FFFFh	Conventional Memory
000A0000h	-	000AFFFFh	Graphics Memory
000B0000h	-	000B7FFFh	Mono Text Memory
000B8000h	-	000BFFFFh	Color Text Memory
000C0000h	-	000CFFFFh	Standard Video BIOS
000D0000h	-	000DFFFFh	Reserved for Extended BIOS
000E0000h	-	000EFFFFh	Extended System BIOS Area
000F0000h	-	000FFFFFh	System BIOS Area (Storage and RAM Shadowing)
Top 0, 1, or 8MB of DRAM			Integrated Graphics Memory
FFE00000h	-	FFFFFFFFh	System Flash

I/O Address Map

Table 3-3 shows the I/O address map.

Table 3-3. I/O Address Map

Address (hex)	Subsystem
0000-000F	Primary DMA Controller
0020-0021	Master Interrupt Controller
0040-0043	Programmable Interrupt Timer (Clock/Timer)
0060	Keyboard Controller
0061	NMI, Speaker control
0063	NMI Controller
0064	Keyboard Controller
0065	NMI Controller
0067	NMI Controller
0070-007F	CMOS RAM, NMI Mask Reg, RT Clock
0080	System reserved
0081-0083	DMA Page Registers
0084-0086	System reserved
0087	DMA Page Register
0088	System reserved
0089-008B	DMA Page Registers
008C-008E	System reserved
008F	DMA Page Register
0090-0091	System reserved
0092	Fast A20 gate and CPU reset
0093-009F	System reserved

Table 3-3. I/O Address Map (Continued)

00A0-00A1	Slave Interrupt Controller
00A2-00BF	System reserved
00C0-00DF	Slave DMA Controller #2
00E0-00EF	System reserved
00F0-00FF	Math Coprocessor
01F0-01F7	IDE Hard Disk Controller
0200-0240h	Mapped to ISA
0240-0260h	Mapped to ISA
0279h	Mapped to ISA
02E8-02EF	Serial Port 4 (COM4)
02F8-02FF	Serial Port 2 (COM2)
0300-0340h	Mapped to ISA
0340-0360h	Mapped to ISA
0378-037F	Parallel Port (Standard and EPP)
03B0-03BB	Video (monochrome)
03C0-03DF	Video (VGA)
03E8-03EF	Serial Port 3 (COM3)
03F0-03F5	Floppy Disk Controller
03F6	IDE Hard Disk Controller
03F7	Floppy Disk Controller
03F8-03FF	Serial Port 1 (COM1)
04D0-04D1	Edge/Level Trigger PIC
0778-077F	Parallel Port (ECP Extensions) (Port 378+400)
0A79h	Mapped to ISA
0CF8-0CFF	PCI Configuration Registers
0CF9	Reset Control Register

Floppy Drive Interface

The SCH3114I-NU (U15) chip provides the floppy controller and supports one floppy drive as configured. The floppy signals are provided through the standard 34-pin header (J17). The floppy controller will support a 360k, 720k, 1.2M, 1.44M, or 2.88M drive.

The floppy drive header uses 34 pins, 2 rows, odd/even sequence (1, 2) with 0.100" pitch.

Parallel Port Interface

Parallel port supports standard parallel, Bi-directional, ECP and EPP protocols. The SCH3114I-NU chip (U15) provides separate parallel port interface signals.

The parallel header uses 26 pins, 2 rows, odd/even sequence (1, 2), with 0.100" pitch.

Table 3-4. Parallel Interface Pin Signals (J16)

Pin #	Signal	In/Out	Description
1	Strobe*	Out	Strobe* – This is an output signal used to strobe data into the printer. I/O pin in ECP/EPP mode.
2	AFD*	Out	Auto Feed* – This is a request signal into the printer to automatically feed one line after each line is printed.
3	PD0	I/O	Parallel Port Data 0 – These pins (0 to 7) provide parallel port data.
4	ERR*	Out	Error* – This is a status output signal from the printer. A Low State indicates an error condition on the printer.
5	PD1	I/O	Parallel Port Data 1 – Refer to pin-3 for more information.
6	INIT*	Out	Initialize* – This signal used to Initialize printer. Output in standard Mode, I/O in ECP/EPP mode.
7	PD2	I/O	Parallel Port Data 2 – Refer to pin-3 for more information.
8	SLIN	Out	Select In – This output signal is used to select the printer. I/O pin in ECP/EPP mode.
9	PD3	I/O	Parallel Port Data 3 – Refer to pin-3 for more information.
10, 12	GND		Ground
11	PD4	I/O	Parallel Port Data 4 – Refer to pin-3 for more information.
13	PD5	I/O	Parallel Port Data 5 – Refer to pin-3 for more information.
14, 16	GND		Ground
15	PD6	I/O	Parallel Port Data 6 – Refer to pin-3 for more information.
17	PD7	I/O	Parallel Port Data 7 – Refer to pin-3 for more information.
18, 20	GND		Ground
19	ACK*	In	Acknowledge* – This printer output status indicates it has received the data and is ready to accept new data if the signal state is Low.
21	BUSY	In	Busy – This printer output status indicates the printer is not ready to accept data if the signal state is High.
22, 24	GND		Ground
23	PE	In	Paper End – The printer output status indicates the printer is out of paper if the signal state is High.
25	SLCT	In	Select – This printer output status indicates the printer is selected and powered on if the signal state is High.
26	Key/NC		Key - Not connected

Note: The shaded areas denote power or ground. The signals marked with * = Negative true logic.

Serial Interfaces

Two MAX213ECAI+ chips and two LTC1334CG#PBF chips provide the circuitry for the four serial ports: The MAX213ECAI+ chips for RS232 mode and the LTC1334CG#PBF chips for RS485/RS422 modes. The four serial ports support the following features:

- Four individual 16550-compatible UARTs
- Programmable word length, stop bits and parity
- 16-bit programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Four individual 16-bit FIFOs
- Serial A Interface (J11)
  - Serial Port 1 (COM1) supports RS232/RS485/RS422 and full modem support
  - Serial Port 2 (COM2) supports RS232/RS485/RS422 and full modem support
- Serial B Interface (J12)
  - Serial Port 3 (COM3) supports RS232/RS485/RS422 and full modem support
  - Serial Port 4 (COM4) supports RS232/RS485/RS422

> **NOTE** The RS232 and RS485/RS422 modes can be selected for any serial port in BIOS Setup under the *Advanced* menu. However, the RS232 mode is the default selection (Standard) for any serial port.

To implement the two-wire RS485 mode on any serial port, you must tie the equivalent pins together for each port.

For example, on Serial Port 1, tie pin 3 to 5 and pin 4 to 6 at the Serial A interface header (J11) as shown in Figure 3-1. As an alternate, tie pin 2 to 3 and pin 7 to 8 at the DB9 serial connector for Serial Port 1 as shown in Figure 3-1. Refer also to the following tables for the specific pin signals on each connector.

> **NOTE** The RS422 mode uses a four-wire interface and does not require any pins tied together, but you must select RS485 in BIOS Setup and make sure the termination jumper is removed.

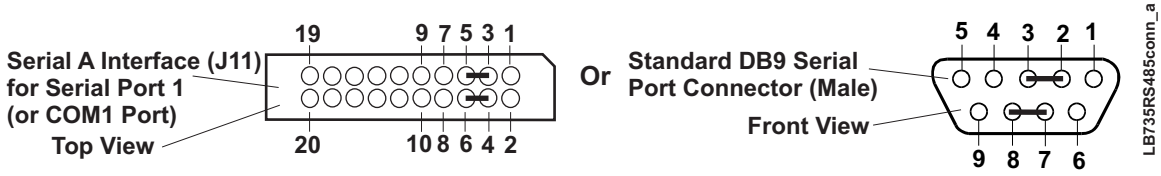

Figure 3-1. RS485 Serial Port Implementation

Table 3-5 defines the pins and corresponding signals for the Serial A interface header (Serial Ports 1 and 2) and Table 3-6 defines the pins and corresponding signals for the Serial B interface header (Serial Ports 3 and 4).

Both Serial A and B headers use 20 pins, 2 rows, odd/even sequence (1, 2) with 0.100" pitch.

Table 3-5. Serial A Interface Pin Signals (J11)

Pin #	Pin # DB9	Signal	Description
1	1 (COM1)	DCD1*	Data Carrier Detect 1 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR1 as part of the DTR/DSR handshake.
2	6	DSR1*	Data Set Ready 1 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR1 for overall readiness to communicate.
3	2	RXD1	Receive Data 1 – Serial port 1 receive data in.
		RX1-	RX1- – If in RS485 or RS422 mode, this pin is Receive Data 1 -.
4	7	RTS1*	Request To Send 1 – Indicates Serial port 1 is ready to transmit data. Used as hardware handshake with CTS1 for low level flow control.
		TX1+	TX1+ – If in RS485 or RS422 mode, this pin is Transmit Data 1 +.
5	3	TXD1	Transmit Data 1 – Serial port 1 transmit data out.
		TX1-	TX1- – If in RS485 or RS422 mode, this pin is Transmit Data 1 -.
6	8	CTS1*	Clear to Send 1 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS1 for low level flow control.
		RX1+	RX1+ – If in RS485 or RS422 mode, this pin is Receive Data 1 -.
7	4	DTR1*	Data Terminal Ready 1 – Indicates this Serial port is powered, initialized, and ready. Used as hardware handshake with DSR1 for overall readiness to communicate.
8	9	RI1*	Ring Indicator 1 – Indicates external serial communications device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	5	GND	Ground
10	NC	KEY/	Key
		NC	Not connected
11	1 (COM2)	DCD2*	Data Carrier Detect 2 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR2 as part of the DTR/DSR handshake.
12	6	DSR2*	Data Set Ready 2 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR2 for overall readiness to communicate.
13	2	RXD2	Receive Data 2 – Serial port 2 receive data in.
		RX2-	RX1- – If in RS485 or RS422 mode, this pin is Receive Data 1 -.
14	7	RTS2*	Request To Send 2 – Indicates Serial port 2 is ready to transmit data. Used as hardware handshake with CTS2 for low level flow control.
		TX2+	TX2+ – If in RS485 or RS422 mode, this pin is Transmit Data 2 +.
15	3	TXD2	Transmit Data 2 – Serial port 2 transmit data out
		TX2-	TX2- – If in RS485 or RS422 mode, this pin is Transmit Data 2 -.

Table 3-5. Serial A Interface Pin Signals (J11) (Continued)

16	8	CTS2* RX2+	Clear To Send 2 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS2 for low level flow control. RX2+ – If in RS485 or RS422 mode, this pin is Receive Data 2 -.
17	4	DTR2*	Data Terminal Ready 2 – Indicates Serial port 1 is powered, initialized, and ready. Used as hardware handshake with DSR2 for overall readiness to communicate.
18	9	RI2*	Ring Indicator 2 – Indicates external serial communications device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
19	5	GND	Ground
20	NC	NC	Not connected

Note: The shaded area denotes power or ground. Signals are listed in the table with RS232 first, followed by RS422/RS485. The signals marked with * = Negative true logic.

Table 3-6. Serial B Interface Pin Signals (J12)

Pin #	Pin # DB9	Signal	Description
1	1 (COM3)	DCD3*	Data Carrier Detect 3 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR3 as part of the DTR/DSR handshake.
2	6	DSR3*	Data Set Ready 3 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR3 for overall readiness to communicate.
3	2	RXD3 RX3-	Receive Data 3 – Serial port 3 receive data in RX3- – If in RS485 or RS422 mode, this pin is Receive Data 3 -.
4	7	RTS3* TX3+	Request To Send 3 – Indicates Serial port 3 is ready to transmit data. Used as hardware handshake with CTS3 for low level flow control. TX3+ – If in RS485 or RS422 mode, this pin is Transmit Data 3 +.
5	3	TXD3 TX3-	Transmit Data 3 – Serial port 3 transmit data out TX3- – If in RS485 or RS422 mode, this pin is Transmit Data 3 -.
6	8	CTS3* RX3+	Clear To Send 3 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS3 for low level flow control. RX3+ – If in RS485 or RS422 mode, this pin is Receive Data 3 -.
7	4	DTR3*	Data Terminal Ready 3 – Indicates this Serial port is powered, initialized, and ready. Used as hardware handshake with DSR3 for overall readiness to communicate.
8	9	RI3*	Ring Indicator 3 – Indicates external serial communications device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	5	GND	Ground
10	NC	KEY	Not Connected

Table 3-6. Serial B Interface Pin Signals (J12) (Continued)

11	1 (COM4)	DCD4*	Data Carrier Detect 4 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR4 as part of the DTR/DSR handshake.
12	6	DSR4*	Data Set Ready 4 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR4 for overall readiness to communicate.
13	2	RXD4 RX4-	Receive Data 4 – Serial port 4 receive data in RX4- – If in RS485 or RS422 mode, this pin is Receive Data 4 -.
14	7	RTS4* TX4+	Request To Send 4 – Indicator to serial output port 4 is ready to transmit data. Used as hardware handshake with CTS4 for low level flow control. TX4+ – If in RS485 or RS422 mode, this pin is Transmit Data 4 +.
15	3	TXD4 TX4-	Transmit Data 4 – Serial port 4 transmit data out TX4- – If in RS485 or RS422 mode, this pin is Transmit Data 4 -.
16	8	CTS4* RX4+	Clear To Send 4 – Indicator to serial port 4 that external serial communications device is ready to receive data. Used as hardware handshake with RTS4 for low level flow control. RX4+ – If in RS485 or RS422 mode, this pin is Receive Data 4 +.
17	4	DTR4*	Data Terminal Ready 4 – Indicates this Serial port is powered, initialized, and ready. Used as hardware handshake with DSR4 for overall readiness to communicate.
18	9	RI4*	Ring Indicator 4 – Indicates external serial communications device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
19	5	GND	Ground
20	NC	NC	Not connected

Note: The shaded areas denote power or ground. Signals are listed in the table with RS232 first, followed by RS485/RS422. The signals marked with * = Negative true logic.

Utility Interfaces

The Utility interfaces consist of two headers that provide the standard interface signals for the following devices:

- Utility 1 (J15)
  - Keyboard
  - External battery connection
  - Reset Switch
  - Speaker
- Utility 2 (J13)
  - PS/2 Mouse
  - SMBus
  - Power button

Utility 1 Interface

The Utility 1 (J15) interface uses a 16-pin connector and provides the various interface signals to an external I/O board with external connections for the respective connectors such as, keyboard, speaker, etc. Table 3-7 provides the pin-outs and interface signals for Utility 1 interface and uses 16 pins, 2 rows, odd/even, (1, 2) with 0.100" pin spacing.

- Keyboard
- Battery
- Reset Switch
- Speaker
- External voltages (+3.3V Out to Power On LED and +5V Power Out to Keyboard)

Keyboard Interface

The signal lines for a PS/2 keyboard are provided through the Utility 1 interface, which is also fully PC/AT compatible.

External Battery

An external battery input connection is provided through a Utility 1 interface for the Real Time Clock's operation in the event the on-board battery is not used.

Reset Switch

The signal lines for a reset switch are provided through the Utility 1 interface.

> **NOTE** To perform the equivalent of a power-on reset, the reset button must be pressed and held for a minimum of three seconds.

Speaker

The signal lines for a speaker port with 0.1-watt drive are provided through a Utility 1 interface (J15).

Table 3-7. Utility 1 Interface Pin Signals (J15)

Pin #	Signal	I/O	Description
1	NC	-	Not connected (-12V Power)
2	GND	I	Ground
3	NC	-	Not connected (-5V Power)
4	GND	I	Ground
5	LED	O	Power-On LED – This on-board +3.3 volts is provided through 330 ohm resistor to an external Power-On LED.
6	NC	-	Not connected (Power Good)
7	SPKR+	O	+ Speaker Output – This signal drives external PC "Beep" speaker.
8	GND	I	Ground
9	RSTSW*	I	Reset Switch – This signal (ground) provided from external reset switch.
10	NC	-	Not connected (Keyboard Switch)
11	KBDATA	I/O	Keyboard Data – Data signal provided to external keyboard connector.
12	KBCLK	I/O	Keyboard Clock – Clock signal provided to external keyboard connector.
13	GND	I	Keyboard Ground
14	KBDPWR	O	Keyboard Power – This +5 volts is provided to external keyboard connector. Requires external fuse for keyboard/mouse protection.
15	BATV+	I	Backup Battery – This connection provides an additional backup battery from an external source. It can also be used in place of the on-board backup battery, B1, shipped with all LittleBoard 735s. Each RTS battery input is protected with a zener diode.
16	BATV-	I	Battery - Return (Grounded)

Note: The shaded areas denote power or ground. The signals marked with * = Negative true logic.

Utility 2 Interface

The Utility 2 (J13) interface consists of a 24-pin header used to route various signals to an external board with external connections, or directly to the respective device such as the mouse and power button. Table 3-9 lists the pin signals of the Utility 2 interface. The J13 header uses 24 pins, 2 rows, odd/even (1, 2) pin sequence with 0.100" (2.54mm) pitch.

- PS/2 Mouse signals
- SMBus signals
- Power button signal

System Management Bus (SMBus)

The I/O Hub, 82801GBM (Southbridge), contains both a host and slave SMBus port but the host cannot access the slave internally. The slave port allows an external master access to the I/O Hub through the header (J13). The master contained in the 82801GBM is used to communicate with the SDRAM DDR2 SODIMM, 82574IT Gigabit Ethernet controller, and the clock generator. Table 3-8 lists the corresponding binary addresses of these devices on the SMBus.

Table 3-8. SMBus Reserved Addresses

Component	Address Binary
SDRAM SODIMM	$1010,000x_b$
Clock Generator (9LPRS501)	$1101,001x_b$
I/O Hub (82801GBM)	$0000,000x_b$ (default) Programmable Master

Mouse Interface

The signal lines for a PS/2 mouse are provided through the Utility 2 interface (J13).

Table 3-9. Utility 2 Interface Pin Signals (J13)

Pin #	Signal	I/O	Description
1	NC	-	Not connected (Lid Switch)
2	PWRBT*	I	Power Button – This signal from an external switch to the I/O Hub is not used with AT Power supplies.
3	BATLOW*		Battery Low – This signal from external battery indicates to the I/O Hub there is insufficient power to boot the system.
4	NC	O	Not connected (IR Mode select)
5	NC	-	Not connected (IR Transmit Data)
6	NC	-	Not connected (IR Receive Data)
7	GND	-	Ground
8	VCC	-	+5 Volts
9	MDATA	I/O	Mouse Data – Data signal provided to external mouse connector.
10	MCLK	I/O	Mouse Clock– Clock signal provided to external mouse connector
11	GND	-	Ground
12	VCC	-	+5 Volts
13	SMBCLK	-	SMBus Clock – Clock signal provided to external devices.
14	SMBDATA	-	SMBus Data – Data signal provided to external devices.
15	NC	-	Not connected (+5V USB Port Power)
16	NC	-	Not connected (+5V USB Port Power)
17	NC	-	Not connected (USB 0 Negative Data Signal)
18	NC	-	Not connected (USB 1 Negative Data Signal)
19	NC	-	Not connected (USB 0 Positive Data Signal)
20	NC	-	Not connected (USB 1 Positive Data Signal)
21	NC	-	Not connected (USB Port ground)
22	NC	-	Not connected (USB Port ground)
23	NC	-	Not connected [USB Port shield (Cable Shield)]
24	NC	-	Not connected [USB Port shield (Cable Shield)]

Note: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

USB Interfaces

The I/O Hub (82801GBM) provides the USB solution for both legacy UHCI controller and EHCI controller (USB 2.0) support. The I/O Hub (Southbridge) contains port-routing logic that determines which controller (UHCI or EHCI) handles the USB data signals. The J44 header provides two of the six USB ports: USB0 and USB1. The J14 header provides USB2 and USB3, and the J39 header provides USB4 and USB5.

USB 2.0 Support

The I/O Hub (Southbridge) contains an Enhanced Host Controller Interface (EHCI) compliant host controller, which supports up to six high-speed USB 2.0 Specification compliant root ports. The higher speed USB 2.0 specification allows data transfers up to 480 Mbps using the same pins as the six full-speed/ low-speed USB UHCI ports. The I/O Hub (Southbridge) port-routing logic determines which of the controllers (UHCI or the EHCI) processes the USB signals.The USB 2.0 features implemented in the USB ports include the following:

- One EHCI host controller for all six USB ports
- Supports USB V2.0 Specification

Legacy USB Support

The I/O Hub (Southbridge) supports three USB Universal Host Controller Interfaces (UHCI) and each Host Controller includes a root hub with two separate USB ports each, for a total of six USB ports. The USB Legacy features implemented in the USB ports include the following:

- Three root hubs for six USB ports
- Support for USB v1.1 and UHCI v1.1 with integrated physical layer transceivers
- Improved arbitration latency for UHCI controllers
- UHCI controllers support Analog Front End (AFE) embedded cell instead of USB I/O buffers to allow for USB high-speed signaling rates
- Three shared over-current fuses, located on the board, are used on all six USB ports

CAUTION	ADLINK does not recommend connecting a USB boot device to the LittleBoard 735 through an external hub. Instead, connect the USB boot device directly to the LittleBoard 735.

USB0 and USB1

Table 3-10 lists the USB0 and USB1 pin signals which use 10 pins, 2 rows, odd/even sequence (1, 2) with 0.079" (2mm) pitch.

Table 3-10. USB 0 & 1 Interface Pin Signals (J44)

Pin #	Signal	Description
1	USBPWR0	+5 volts power, USB 0
2	USBPWR1	+5 volts power, USB 1
3	USB0-	USB 0 Data Negative
4	USB1-	USB 1 Data Negative
5	USB0+	USB 0 Data Positive
6	USB1+	USB 1 Data Positive
7	USB GND0	USB 0 Ground
8	USB GND1	USB 1 Ground

Table 3-10. USB 0 & 1 Interface Pin Signals (J44) (Continued)

9	USB GND0	USB 0 Ground
10	USB GND1	USB 1 Ground

Note: The shaded areas denote power or ground.

USB2 and USB3

Table 3-11 lists the USB2 and USB3 pin signals which use 10 pins, 2 rows, odd/even sequence (1, 2) with 0.079" (2mm) pitch.

Table 3-11. USB 2 & 3 Interface Pin Signals (J14)

Pin #	Signal	Description
1	USBPWR2	+5 volts power, USB 2
2	USBPWR3	+5 volts power, USB 3
3	USB2-	USB 2 Data Negative
4	USB3-	USB 3 Data Negative
5	USB2+	USB 2 Data Positive
6	USB3+	USB 3 Data Positive
7	USB GND2	USB 2 Ground
8	USB GND3	USB 3 Ground
9	USB GND2	USB 2 Ground
10	USB GND3	USB 3 Ground

Note: The shaded areas denote power or ground.

USB4 and USB5

Table 3-12 lists the USB4 and USB5 pin signals which use 10 pins, 2 rows, odd/even sequence (1, 2) with 0.079" (2mm) pitch.

Table 3-12. USB 4 & 5 Interface Pin Signals (J39)

Pin #	Signal	Description
1	USBPWR4	+5 volts power, USB 4
2	USBPWR5	+5 volts power, USB 5
3	USB4-	USB 4 Data Negative
4	USB5-	USB 5 Data Negative
5	USB4+	USB 4 Data Positive
6	USB5+	USB 5 Data Negative
7	USB GND4	USB 4 Ground
8	USB GND5	USB 5 Ground
9	USB GND4	USB 4 Ground
10	USB GND5	USB 5 Ground

Note: The shaded areas denote power or ground.

Audio Interface

The audio solution on the LittleBoard 735 is provided by the Realtek ALC203-LF audio CODEC. The chip is defined by AC97 and is revision 2.2 compliant. The audio interface signals are supplied to the 26-pin 2mm connector (J9). Refer to the following list for the *Audio CODEC* (ALC203-LF) features.

- Analog Mixer Dynamic Range 97dB (typ)
- D/A Dynamic Range 89dB (typ) and A/D Dynamic Range 90dB (typ)
- AC'97 Rev 2.1 compliant
- High quality Sample Rate Conversion (SRC) from 4kHz to 48kHz
- 3D Sound circuitry and PC-Beep passthrough to Line Out while reset is held active low
- True Line Level Output with volume control independent of Line Out

Table 3-13 describes the pin signals of the audio interface which uses 26 pins, 2 rows, odd/even sequence (1, 2) with 0.079" (2mm) pitch.

Table 3-13. Audio Interface Pin Signals (J9)

Pin #	Signal	Description
1	NC	Not connected (Video Audio In signal left channel)
2	VIDEO_GND	Video Audio ground
3	NC	Not connected (Video Audio In signal right channel)
4	CD_L	CD-ROM signal left channel
5	CD_GND	CD-ROM Audio ground
6	CD_R	CD-ROM signal right channel
7	LINE_IN_L	Line In signal left channel
8	LINE_IN_GND	Line In Audio ground
9	LINE_IN_R	Line In signal right channel
10	MIC1	Microphone In signal 1 or left channel
11	MIC_GND	Microphone Audio ground
12	MIC2	Microphone In signal 2 or right channel
13	MIC_REF	Microphone reference signal
14	NC/KEY	Not Connected - Key
15	PHONE_IN	Phone signal In
16	PHONE_GND	Phone Audio ground
17	MONO_OUT	Monaural signal Out
18	MONO_GND	Monaural Audio ground
19	+AOUT_L	+ Audio Out signal Left channel
20	-AOUT_L	- Audio Out Left ground
21	+AOUT_R	+ Audio Out signal Right channel
22	-AOUT_R	- Audio Out Right ground
23	GND	Audio Ground (tied to all audio grounds)
24	HP_L	Headphone signal Left channel
25	HP_R	Headphone signal Right channel
26	NC	Not Connected (Headphone In)

Note: The shaded areas denote power or ground.

Video Interfaces

The 82945GSE chip provides the graphics control and video signals to the traditional glass CRT monitors and LCD flat panel displays. The chip features are listed below:

CRT features:

- Support for an integrated 400-MHz, 24-bit RAMDAC to drive a progressive scan analog monitor and outputs to three, 8-bit DACs that provide the R, G, and B signals to the monitor
- Support for resolutions up to QXGA (2048x1536)
- Support for a maximum allowable video frame buffer size of 224MB UMA (Unified Memory Architecture)

LVDS Flat Panel features:

- Support for an integrated dual channel LFP Transmitter interface
- Support for LVDS LCD panel resolutions up to UXGA(1600X1200)
- Support for a maximum pixel format of 18 bpp with SSC supported frequency range from 25 MHz to 112 MHz (single channel/dual channel)

TV Out features:

- Support for three integrated 10-bit DACS
- Support for overscaling
- Provide NTSC/PAL
- Provide component, s-video, and composite output interfaces
- Support HDTV: 480p/720p/1080i/1080p

CRT Interface

Table 3-14 describes the pin signals of the CRT interface, which uses 12 pins, 2 rows, odd/even sequence (1, 2) with 0.079" (2mm) pitch.

Table 3-14. CRT Interface Pin Signals (J3)

Pin #	Signal	Description
1	RED	Red – This is the Red analog output signal to the CRT.
2	GND	Ground (Red Return)
3	GREEN	Green – This is the Green analog output signal to the CRT.
4	GND	Ground (Green Return)
5	BLUE	Blue – This is the Blue analog output signal to the CRT.
6	GND	Ground (Blue Return)
7	HSYNC	Horizontal Sync – This signal is used for the digital horizontal sync output to the CRT.
8	GND	Ground
9	VSYNC	Vertical Sync – This signal is used for the digital vertical sync output to the CRT.
10	PWR	Power – Provided through fuse (F1) to +5 volts +/- 5%. F1 is next to J3 connector on board.
11	SDA	DDC (Display Data Channel) Data
12	SCL	DDC (Display Data Channel) Clock

Note: The shaded areas denote power or ground.

LVDS Interface

Table 3-15 describes the pin signals of the LVDS interface, which uses 30 pins, 2 rows, odd/even sequence (1, 2) with 0.079" (2mm) pitch.

Table 3-15. LVDS Interface Pin Signals (J26)

Pin #	Signal	Description	Line	Channel
1	+12V	+12 volt input	NA	NA
2	+VCC (+3.3V/+5V)	JP1 determines voltage on pin		
3	GND	Ground		
4	GND	Ground		
5	LBCLK_P	Clock Positive Output	Clock	Channel 2
6	LBCLK_N	Clock Negative Output		
7	Not Supported	N/A	N/S	
8	Not Supported	N/A		
9	LBDATA2_P	Data Positive Output	2	
10	LBDATA2_N	Data Negative Output		
11	LBDATA1_P	Data Positive Output	1	
12	LBDATA1_N	Data Negative Output		
13	LBDATA0_P	Data Positive Output	0	
14	LBDATA0_N	Data Negative Output		
15	LVDS_BKLT_CTL	Control Panel Backlight	NA	NA
16	LVDD_EN	Enable Panel Power	NA	NA
17	LACLK_P	Clock Positive Output	Clock	Channel 1
18	LACLK_N	Clock Negative Output		
19	Not Supported	N/A	N/S	
20	Not Supported	N/A		
21	LADATA2_P	Data Positive Output	2	
22	LADATA2_N	Data Negative Output		
23	LADATA1_P	Data Positive Output	1	
24	LADATA1_N	Data Negative Output		
25	LADATA0_P	Data Positive Output	0	
26	LADATA0_N	Data Negative Output		
27	L_DDC_CLK	Display Data Channel Clock	NA	NA
28	L_DDC_DAT	Display Data Channel Data	NA	NA
29	LVDS_BKLT_EN	Enable Backlight Inverter	NA	NA
30	NC	Not Connected	NA	NA

Note: The shaded areas denote power or ground.

NOTE Pins 5-14 constitute 2nd channel interface of two channels. Pins 15-26 constitute 1st channel interface of two channels, or a single channel interface.

TV-Out Interface

Table 3-16 describes the pin signals of the TV-Out interface, which uses 6 pins, 2 rows, odd/even sequence (1, 2) with 0.100" (2.54mm) pitch.

Table 3-16. TV-Out Pin Signals (J36)

Pin #	Signal	Description
1	TVDAC A	**TVDAC Channel A Output:** TVDAC_A supports the following: **Composite**: CVBS signal **Component**: Chrominance (Pb) analog signal
2	TV_GND	Ground
3	TVDAC B	**TVDAC Channel B Output:** TVDAC_B supports the following: **S-Video**: Luminance analog signal **Component**: Luminance (Y) analog signal
4	TV_GND	Ground
5	TVDAC C	**TVDAC Channel C Output:** TVDAC_C supports the following: **S-Video**: Chrominance analog signal **Component**: Chrominance (Pr) analog signal
6	TV_GND	Ground

Note: The shaded areas denote power or ground.

Power Interfaces

Power-In Interface

The LittleBoard 735 uses five separate voltages on the board, but only one of the voltages is provided externally (+5 volts) through the external header (J19), which uses a 7-pin vertical header with 0.156" (3.96mm) pitch. Holes for a right angle mounting header are also available at J19. All the onboard voltages are derived from the externally supplied +5 volts DC +/- 5%. The onboard voltages include the CPU core voltages as well as the other voltages used on the board.

Table 3-17 lists the pin signals for the J19 power supply input header, which uses 7 pins, single row with 0.156" (3.96mm) pitch.

Table 3-17. Power Supply Input Pin Signals (J19)

Pin #	Signal	Description
1	+5V	+5.0 Volts – This +5.0 volts DC +/- 5% is the only voltage required for operation.
2	GND	Ground
3	GND	Ground
4	+12V	+12 Volts – This +12 volts is for the PC/104, PC/104-Plus, and LVDS power only.
5	+3.3V	+3.3 Volts – This +3.3 volts is for PC/104-Plus Bus power only (optional).
6	GND	Ground
7	+5V	+5.0 Volts – This +5.0 volts DC +/- 5% is the only voltage required for operation.

Note: The shaded areas denote power or ground. The +12V and +3.3V on the Power Supply Input header (J19) are used for the PCI, ISA bus, and LVDS power, which are supplied externally and not generated on the LittleBoard 735. The -5V and -12V used for the PC/104 bus are supplied through the PC/104 bus or from an external power supply through the Utility 1 header (J15).

ATX Power Interface

Table 3-18 lists the pin signals for the J30 Power-On header, which uses 3 pins, single row with 0.100" (2.54mm) pitch.

Table 3-18. ATX Power Header Pin Signals (J30)

Pin #	Signal	Description
1	PS_ON*	Power Supply On – This signal is sent to the ATX power supply by the LittleBoard 735 to turn On the ATX power supply. This signal can also be used to turn Off the ATX power supply or go into a suspended or standby state.
2	GND	Ground
3	VCC5_ATX_STBY	+5V suspend voltage (+5V, 500mA Standby) – This voltage is supplied from ATX power supply. This voltage is required for normal operation.

Note: The shaded areas denote power or ground. The signals marked with * = Negative true logic.

NOTE If the +5V suspend voltage is not present on the Power On connector (J30, pin 1) the LittleBoard 735 will not completely power on. The board will have power (+5V), but it will not start the boot process and will never completely power up.

Power-On Button Interface

A Power-On Button signal is provided by connecting ground to pin-1 on this header (J46). A Reset Switch signal is provided by connecting ground to pin 3 on this header.

Table 3-19 lists the pin signals for the J46 Power On Button header, which uses 5 pins, single row with 0.100" (2.54mm) pitch.

Table 3-19. Power-On Button Interface Pin Signals (J46)

Pin #	Signal	Description
1	PWRON	Power-On Button input (connect between pins 1 & 2)
2	GND	Ground
3	RST_SW	Reset Switch input or output (connect between pins 3 & 2)
4	NC	Not Connected
5	NC	Not Connected

Note: The shaded area denotes power or ground.

Miscellaneous

Real Time Clock (RTC)

The LittleBoard 735 contains a Real Time Clock (RTC). The BIOS (CMOS) RAM is backed up with a Lithium Battery. If the battery is not present, the BIOS has a battery-free boot option to complete the boot process.

Temperature Monitoring

The Intel Atom processor supports the THERMTRIP# signal for catastrophic thermal protection. The THERMTRIP# is an open drain signal from the processor which is used to shut down the processor core voltage. This signal is connected to the THERMTRIP# input signal and indicates that a thermal trip from the processor occurred and the ICH7-M will immediately transition to the S5 state.

NOTE	The LittleBoard 735 requires a heatsink for the Atom N270 processor.

User GPIO Signals

The LittleBoard 735 provides GPIO pins for custom use. The signals are routed to the J40 header, and the Enable and Initialize values are set in the BIOS. An example of how to use the GPIO pins resides in the Miscellaneous Source Code Examples on the LittleBoard 735 Support Software QuickDrive™.

The example program can be built by using the *make.bat* file. This produces a 16-bit DOS executable application, *gpio.exe*, which can be run on the LittleBoard 735 to demonstrate the use of GPIO pins. For more information about the GPIO pin operation, refer to the Programming Manuals for the Southbridge (82801GBM) and Super I/O (SCH3114I-NU) controllers at:

http://www.intel.com/assets/pdf/datasheet/307013.pdf

http://www.smsc.com/main/catalog/sch311x.html

Table 3-20 lists the pin signals for the J40 GPIO header, which uses 10 pins, two rows, odd/even sequence with 0.079" (2mm) pitch.

Table 3-20. User GPIO Pin/Signal Descriptions (J40)

Pin #	Signal	Description
1	VCC	+3.3 Volts DC +/ 5%
2	GND	Ground
3	GPI0	User defined
4	GPO0	User defined
5	GPI1	User defined
6	GPO1	User defined
7	GPI2	User defined
8	GPO2	User defined
9	GPI3	User defined
10	GPO3	User defined

Note: The shaded areas denote power or ground.

SMBus Interface

Table 3-21 lists the pin signals for the J45 SMBus Reset header, which uses 5 pins, single row, and 0.49" pitch.

Table 3-21. SMBus Pin/Signal Descriptions (J45)

Pin #	Signal	Description
1	SCL	SMBus Clock Reset
2	GND	Ground
3	SDA	SMBus Data Reset
4	VCC	+3.3 Volts DC +/ 5%
5	ALERT	SMBus Alert

Note: The shaded areas denote power or ground.

Oops! Jumper (BIOS Recovery)

The Oops! jumper is provided in the event the BIOS settings you have selected prevent you from booting the system. By using the Oops! jumper you can prevent the current BIOS settings in the EEPROM from being loaded, forcing the use of the default settings. Connect the DTR pin to the RI pin on serial port 1 (COM 1) prior to boot up to prevent the present BIOS settings from loading. After booting with the Oops! jumper in place, remove the Oops! jumper and go into BIOS Setup. Change the desired BIOS settings, or select the default settings, and save changes before rebooting the system.

To convert the Serial A interface to an Oops! jumper, short together the DTR (7) and RI (8) pins on Serial A (J11) header for Serial Port 1. As an alternate, short the equivalent pins, 4 and 9, on the Serial Port 1 DB9 connector as shown in Figure 3-2.

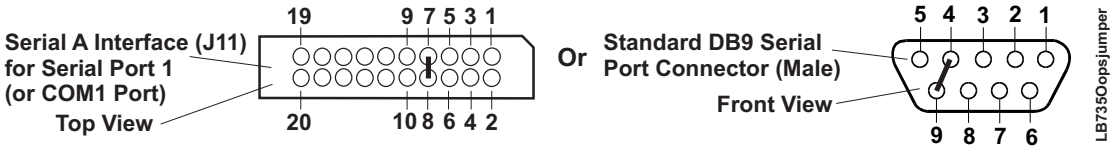

Figure 3-2. Oops! Jumper Connection

Serial Console

The LittleBoard 735 supports the serial console (or console redirection) feature. This I/O function is provided by an ANSI-compatible serial terminal, or the equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display.

Serial Console Setup

The serial console feature is implemented by connecting a standard null modem cable or modified serial cable (or “Hot Cable”) between one of the serial ports, such as Serial 1 (J11A) and the serial terminal, or a PC with communications software. The BIOS Setup Utility controls the serial console settings on the LittleBoard 735. Refer to Chapter 4, BIOS Setup for the settings of the serial console option, the serial terminal, or PC with communications software and the connection procedure.

Hot (Serial) Cable

To convert a standard serial cable to a Hot Cable, specific pins must be shorted together at the Serial port connector or at the DB9 cable connector. For example, short the RTS (7) and RI (9) at the rear of the respective DB9 cable connector as shown in Figure 3-3.

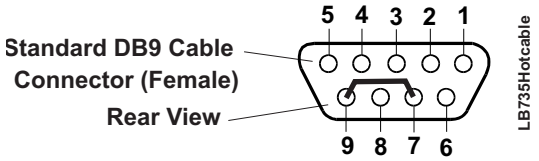

Figure 3-3. Hot Cable Jumper

Watchdog Timer

The watchdog timer (WDT) restarts the system if a mishap occurs, ensuring proper start-up after the interruption. Possible problems include failure to boot properly, the application software's loss of control, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT (watchdog timer) can be used both during the boot process and during normal system operation.

- During the Boot process – If the operating system fails to boot in the time interval set in the BIOS, the system will reset.

  Enable the WDT in Boot Settings Configuration of BIOS Setup. Set the WDT for a time-out interval in seconds, between 1 and 255, in one-second increments in the Boot Setting Configuration screen. Ensure you allow enough time for the boot process to complete and for the OS to boot. The OS or application must tickle the WDT as soon as it comes up. This can be done by accessing the hardware directly or through a BIOS call.

- During System Operation – An application can set up the WDT hardware through a BIOS call, or by accessing the hardware directly. Some ADLINK Board Support Packages provide an API interface to the WDT. The application must tickle the WDT in the time set when the WDT is initialized or the system will be reset. You can use a BIOS call to tickle the WDT or access the hardware directly.

  The BIOS implements interrupt 15 function 0C3h to manipulate the WDT.

- Watchdog Code examples – ADLINK has provided source code examples on the LittleBoard 735 Support Software CD-ROM illustrating how to control the WDT. The code examples can be easily copied to your development environment to compile and test the examples, or make any desired changes before compiling. Refer to the WDT Readme file on the LittleBoard 735 Support Software QuickDrive.

Optional CPU Fan

Table 3-22 lists the pin signals of the optional CPU Fan, which uses 3 pins, single row, with 0.100" (2.54mm) pitch.

Table 3-22. Optional CPU Fan (J34)

Pin #	Signal	Description
1	Fan_Tach	Fan Tachometer – This signal indicates Fan speed
2	VCC	+5.0 volts DC +/- 5%
3	GND	Ground and Modulation

Note: The shaded areas denote power or ground.

Battery Input

Table 3-23 lists the pin signals of the External Battery Input header, which uses 2 pins, single row, with 0.049" (1.24mm) pitch.

Table 3-23. External Battery Input Header (J35)

Pin #	Signal	Description
1	VCC	+5.0 volts DC +/- 5%
2	GND	Ground

Note: The shaded areas denote power or ground.

Chapter 4 BIOS Setup

Introduction

This section assumes the user is familiar with BIOS Setup and does not attempt to describe the inner workings of BIOS functions. Refer to the appropriate PC reference manuals for information about the on-board, ROM-BIOS software interface. If ADLINK has added to or modified the standard functions, these functions will be described.

Entering BIOS Setup (VGA Display)

To enter BIOS Setup using a VGA display for the LittleBoard 735:

1. Turn on the VGA monitor and the power supply to the LittleBoard 735.
2. Start Setup by pressing the [Del] key, when the following message appears on the boot screen.

```
Press DEL to run Setup
```

> **NOTE** If the setting for *Memory Test* is set to Fast, you may not see this prompt appear on screen if the monitor is too slow to display it on start up. If this happens, press the <Del> key early in the boot sequence to enter BIOS Setup.

3. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen.
4. Follow the instructions at the bottom of each screen to navigate through the selections and modify any settings.

Entering BIOS Setup (Serial Console)

Entering the BIOS Setup, in serial console mode, is very similar to the steps you use to enter BIOS Setup with a VGA display, except the actual keys you use.

1. Set the serial terminal, or the PC with communications software to the following settings:
   - 115k baud
   - 8 bits
   - One stop bit
   - No parity
   - No hardware handshake
2. Connect the serial console, or the PC with serial terminal emulation, to Serial Port 1 or Serial Port 2 of the LittleBoard 735.
   - If the BIOS option, *Serial Console* is set to [Enable], use a standard null-modem serial cable.
   - If the BIOS option, *Serial Console* is set to [Hot Cable], use the modified serial cable described in Chapter 3, under *Hot (Serial) Cable*.
3. Turn on the serial console or the PC with serial terminal emulation and the power supply to the LittleBoard 735.
4. Start Setup by pressing the Ctl–c keys, when the following message appears on the boot screen.

```
Hit ^C if you want to run SETUP
```

5. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen.

> **NOTE** The serial console port is not hardware protected, and is not listed in the COM table within BIOS Setup. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

PCI-ISA Bridge Mapping

The LittleBoard 735 supports ISA bus based modules with an on-board PCI-ISA bridge. The PCI-ISA bridge optionally maps the following resources to ISA based modules:

- Memory
- I/O Ports
- IRQs
- DMA Channels

The LittleBoard 735 system BIOS maps the above resources based on information provided in the BIOS Setup screens. By default, only some of the I/O ports are mapped to ISA modules and any memory, IRQs or DMA channels to be mapped to ISA modules must be explicitly specified by the user in the BIOS Setup screens.

The IRQs and DMA channels are mapped with the “PCIPnP/IRQx” fields in BIOS setup (where x specifies the IRQ number.) The IRQs 3, 4, 5, 7, 9, 10, 11, 14, and 15 can be mapped to ISA based modules by changing the default setting for these IRQs from “Available” to “Reserved”.

ISA I/O ports, Memory, and DMA channels can be mapped to ISA modules on the “Boot/Boot Settings Configuration” BIOS setup screen. Six I/O port “windows” and four memory “windows” are available for mapping I/O Port or Memory regions to ISA modules by specifying the window length and base address.

By default, the following I/O port windows are mapped to ISA modules:

- 200-240h
- 240-260h
- 279h
- 300-340h
- 340-360h
- A79h

> **NOTE** 279h and A79 are the ISA PnP ports used by the BIOS and an OS that supports this feature to recognize ISA PnP (Plug and Play) cards.

By default, no memory windows are mapped to ISA modules.

Any of the DMA channels 0, 1, 2, 3, 5, 6, 7 can be mapped to ISA modules by changing the default setting of “LPC Bridge” to “ISA Bridge”.

For example, to configure an ISA Soundblaster PnP card with resources 220/5/1/5 (Port/IRQ/DMA/DMA) so that the Soundblaster would work in Windows XP, the following BIOS Setup changes would be required:

- ISA I/O Ports – no changes necessary. 220h is already mapped to ISA by default.
- IRQ – set IRQ5 to “Reserved” in BIOS Setup. See the paragraph above on mapping IRQs.
- DMA1 and DMA5 – set DMA Channels 1 and 5 to “ISA Bridge” in BIOS Setup. See paragraph above on mapping DMA Channels.

Logo Screen Utility (Splash Screen)

The LittleBoard 735 BIOS supports a graphical logo utility, which can be customized by the user and displayed when enabled through the BIOS Setup Utility. The graphical image can be a company logo or any custom image the user wants to display during the boot process. The custom image can be displayed as the first image displayed on screen during the boot process and remain there, depending on the options selected in BIOS Setup, while the OS boots.

Logo Screen Image Requirements

The user's image may be customized with any standard image editing tool.

The LittleBoard 735 logo screen utility supports the following image formats:

- Bitmap image
- Exactly 640 x 480 pixels
- Exactly 16 colors

> **NOTE** For procedures on loading custom images, see the logo screen utility document available on the ADLINK website.

- Bitmap image
  - 16-Color, 640x480 pixels
  - 256-Color, 640x480 pixels
- JPG image
  - 16-Color, 640x480 pixels
- PCX image
  - 256-Color, 640x480 pixels
- A file size no larger than the sample image

> **NOTE** For procedures on loading custom images, see the OEM Logo Utility document available on the ADLINK web site.

Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed in the Table A-1 below. Requests for support through the Ask an Expert web page are given the highest priority, and usually will be addressed within one working day.

- ADLINK Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the ADLINK web site at http://adlinktech.custhelp.com. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.
- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered followed by an e-mail response. Once you have submitted your request, you must log in to My Stuff where you can check status, update your request, and access other features.
- InfoCenter – This service is also free and available 24 hours a day at the ADLINK web site at http://www.adlinktech.com. However, you must sign up online before you can log in to access this service. The InfoCenter was created as a resource for embedded system developers to share ADLINK'S knowledge, insight, and expertise. This page contains links to White Papers, Specifications, and additional technical information.

Table A-1. Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://adlinktech.custhelp.com
Web Site	http://www.adlinktech.com
Standard Mail	ADLINK Technology, Incorporated 5215 Hellyer Avenue San Jose, CA 95138-1007, USA

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